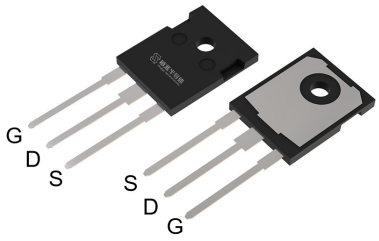
V_{DS}	1200	V
$R_{DS(on),TYP}$@ V_{GS}=20 V	42	mΩ
$I_{D(Silicon\ limited)}$	55	A

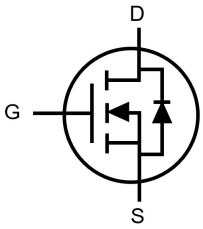
Features

- SiC MOSFET technology
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Very low switching losses
- Low reverse recovery (Qrr)
- 100% Avalanche tested,100% Rg tested

Pb-Free RoHS HF Halogen-Free

TO-247





Part ID	Package Type	Marking	Packing
HCCW120R040H1	TO-247	120R040H1	30pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		1200	V
V_{GSmax}	Gate-Source voltage (dynamic) AC (f >1 Hz) ①		-10/+25	V
V_{GSop}	Gate-Source voltage (static) ②		-5/+20	V
I_D	Continuous drain current @VGS=20V (Silicon limited)	T_C = 25°C	55	A
I_D	Continuous drain current @VGS=20V (Silicon limited)	T_C = 100°C	39	A
I_{DM}	Pulse drain current tested,VGS=20V ③	T_C = 25°C	130	A
EAS	Maximum avalanche energy, single pulsed ④		1620	mJ
P_D	Maximum power dissipation ⑤	T_C = 25°C	259	W
		T_C = 100°C	129	W
T_{STG}	Storage temperature range		-55 to 150	°C
T_J	Operating junction temperature		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑥	0.48	0.58	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑦	32	38	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=100μA	1200	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=1200V,V_{GS}=0V	--	--	50	μA
	Zero gate voltage drain current(Tj=125℃)⑧	V_{DS}=1000V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=-5V,V_{DS}=0V	--	--	-100	nA
I_{GSS}	Gate-body leakage current	V_{GS}=20V,V_{DS}=0V	--	--	100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=10mA	1.8	3	4.5	V
$R_{DS(on)}$	Drain-source on-state resistance ⑨	V_{GS}=20V, I_D=40A	--	42	53	mΩ
		Tj=100℃ ⑧	--	49	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑧	V_{DS}=800V,V_{GS}=0V, f=100kHz	--	2275	--	pF
Coss	Output capacitance ⑧		--	150	--	pF
Crss	Reverse transfer capacitance ⑧		--	10	--	pF
Rg	Gate resistance	f=1MHz	--	1.5	--	Ω
Qg	Total gate charge ⑧	V_{DS}=800V,I_D=40A, V_{GS}=-5/20V	--	105	--	nC
Qgs	Gate-source charge ⑧		--	40	--	nC
Qgd	Gate-drain charge ⑧		--	28	--	nC
Switching Characteristics ⑧						
Td(on)	Turn-on delay time	V_{DD}=800V, I_D=40A, R_G=12Ω, V_{GS}=-5/20V L=2.2mH (Fig17)	--	22	--	ns
Tr	Turn-on rise time		--	35	--	ns
Td(off)	Turn-off delay time		--	44	--	ns
Tf	Turn-off fall time		--	49	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=-5V	--	4.2	6	V
Trr	Reverse recovery time ⑧	V_{DD}=800V I_{sd}=40A, V_{GS}=0V di/dt=500A/μs	--	25	--	ns
Qrr	Reverse recovery charge ⑧		--	86	--	nC
Irrm	Peak Reverse Recovery Current ⑧		--	6	--	A

NOTE:

① When using MOSFET Body Diode VGSmax = -10V/+25V

② MOSFET can also safely operate at -5/+20 V

③ Single pulse; pulse width limited by max junction temperature.

④ This maximum value is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} =20V； 100% FT tested at L = 10mH, I_{AS} = 12A.

⑤ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

⑥ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑦ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑧ Guaranteed by design, not subject to production testing.

⑨ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

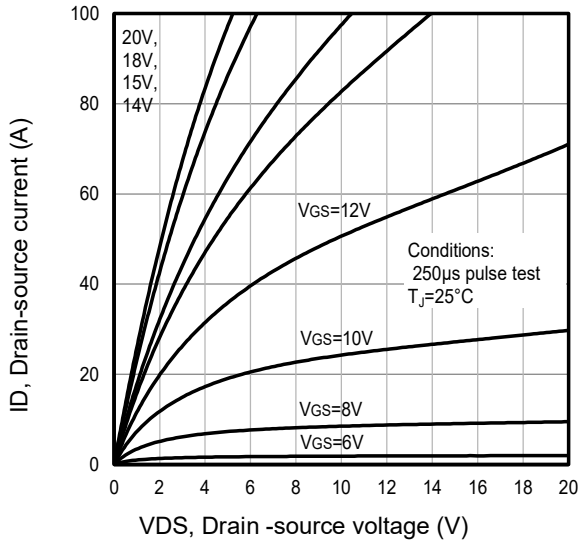


Fig1. Typical output characteristics

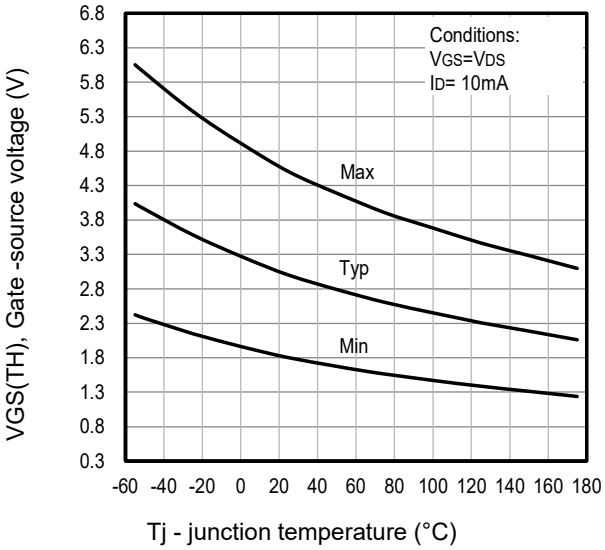


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

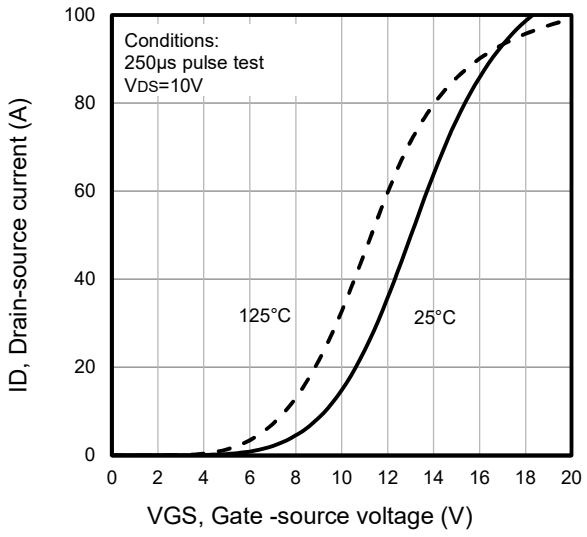


Fig3. Typical transfer characteristics

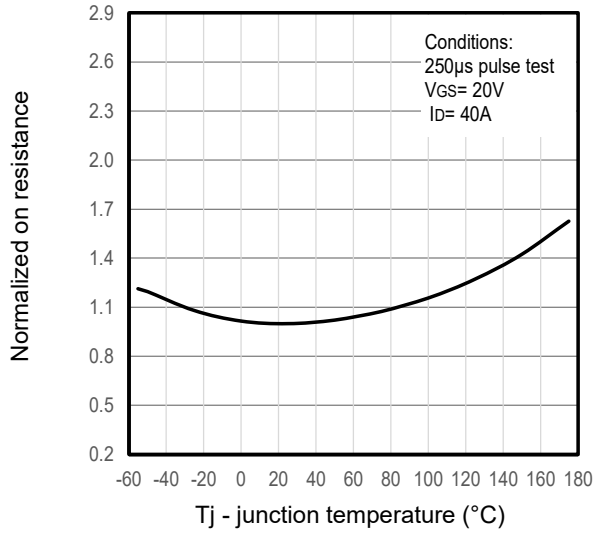


Fig4. Typical normalized on-resistance Vs. Tj

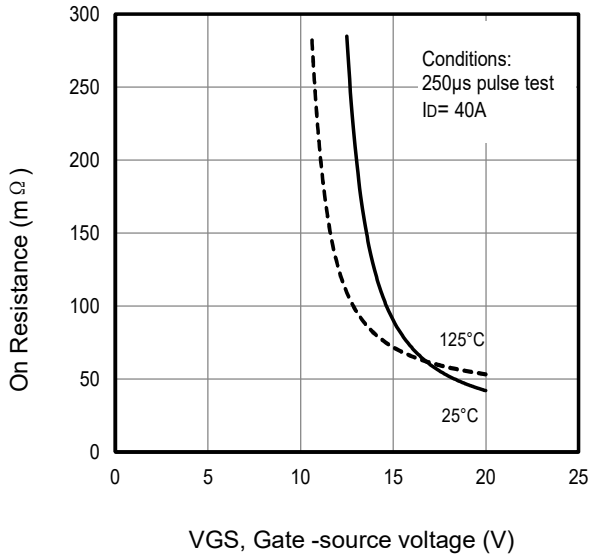


Fig5. Typical on resistance Vs gate -source voltage

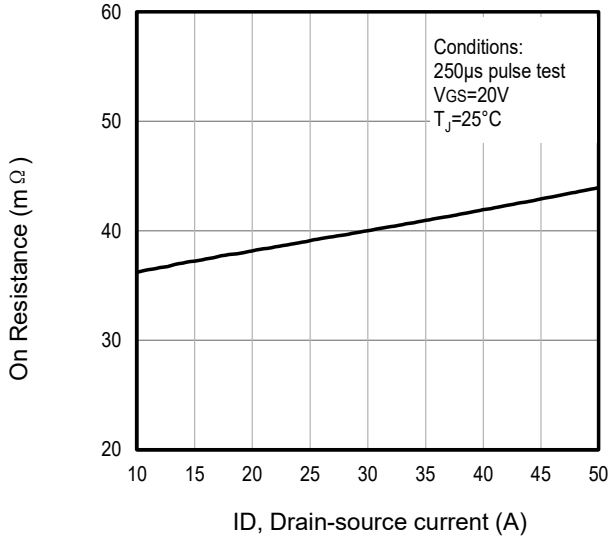


Fig6. Typical on resistance Vs drain current

Typical Characteristics

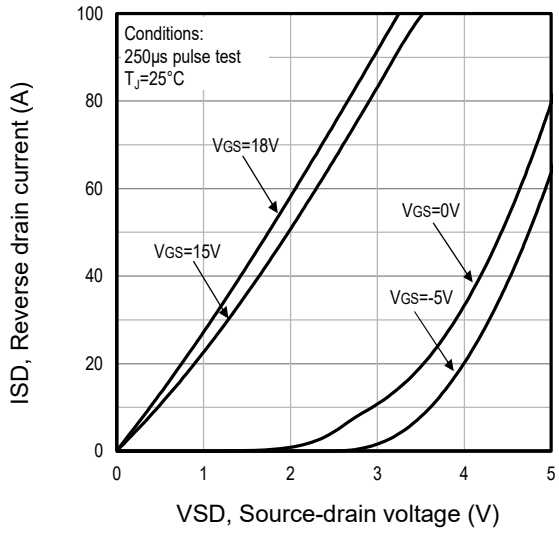


Fig7. Typical source-drain diode forward voltage

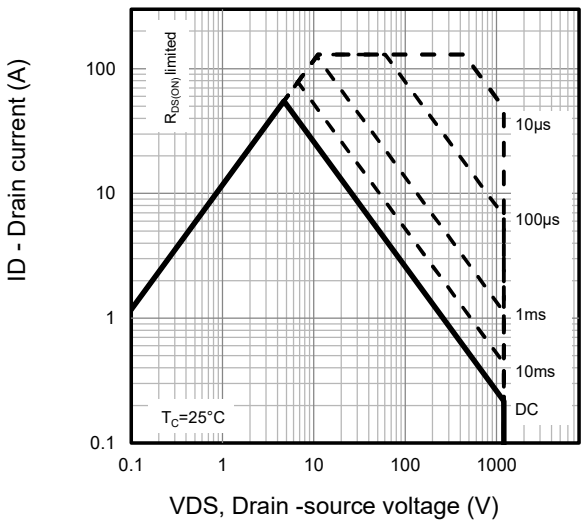


Fig8. Maximum safe operating area

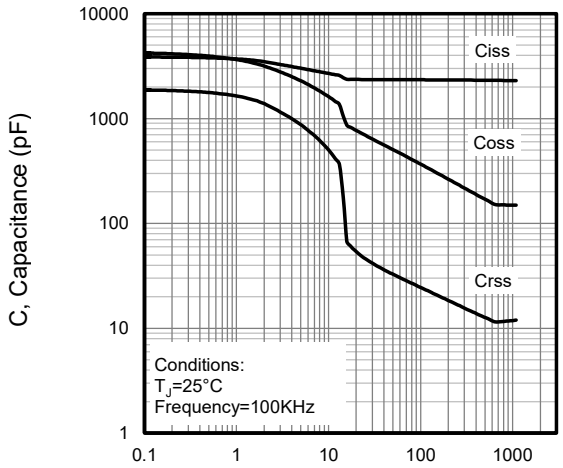


Fig9. Typical capacitance Vs. drain-source voltage

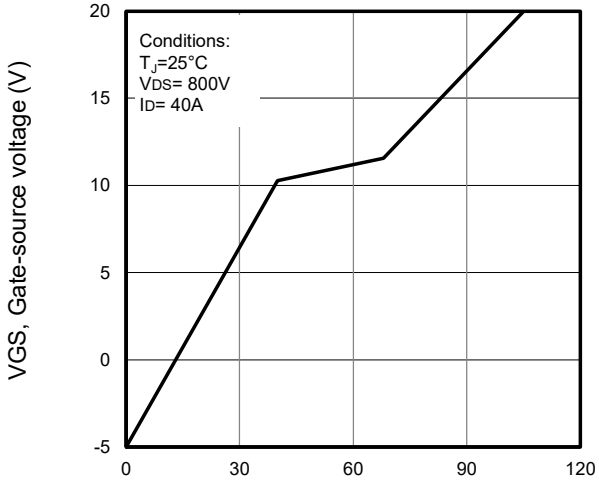


Fig10. Typical gate charge Vs. gate-source voltage

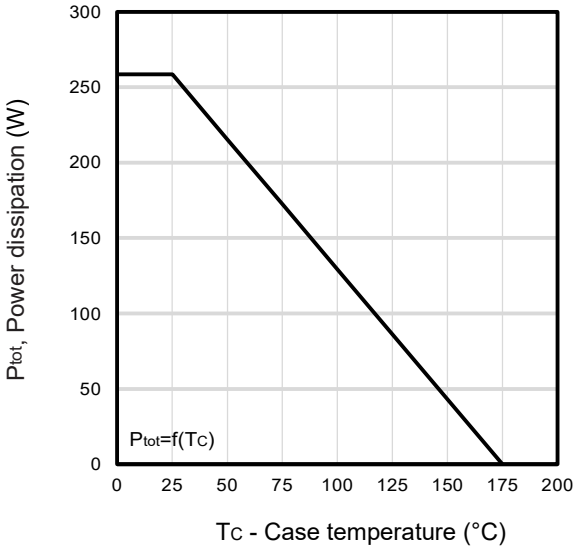


Fig11. Power dissipation Vs. case temperature

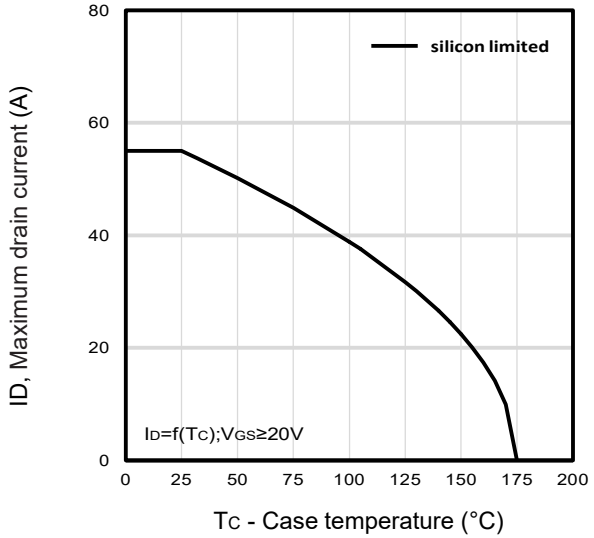


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

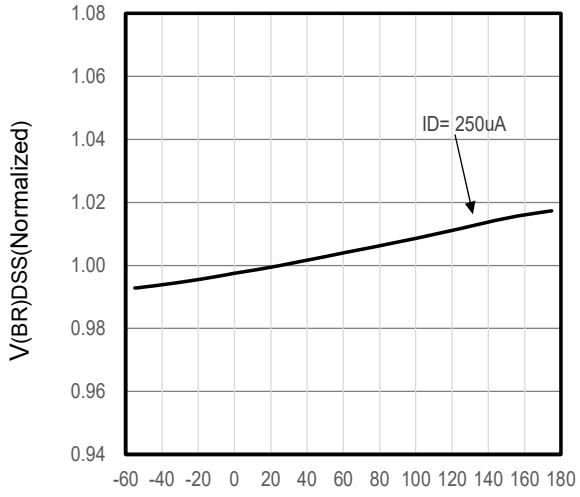


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

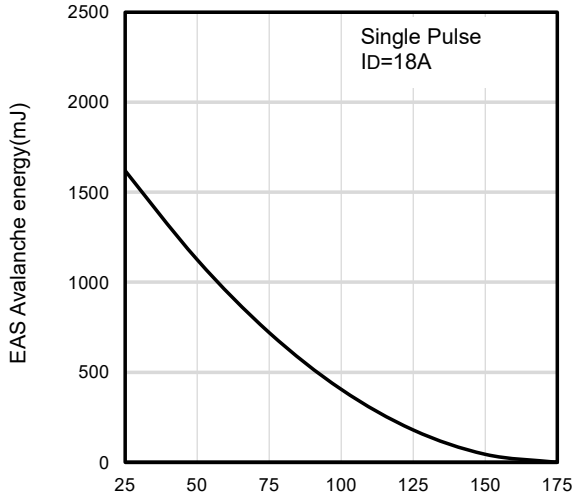


Fig14. Maximum avalanche energy vs temperature (°C)

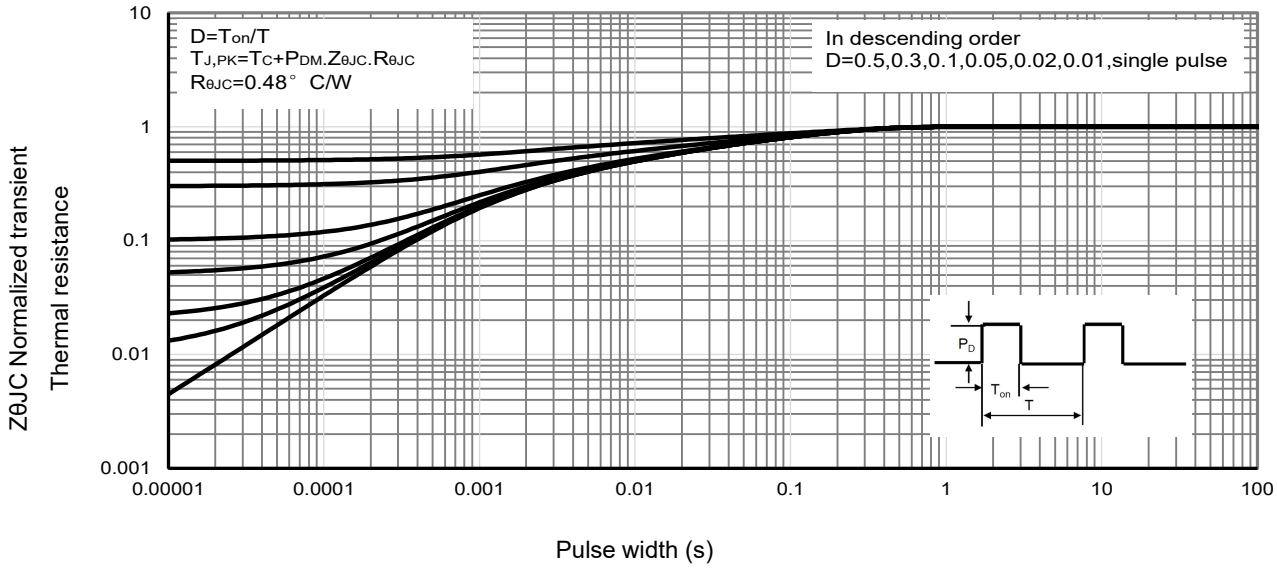


Fig15 . Normalized maximum transient thermal impedance

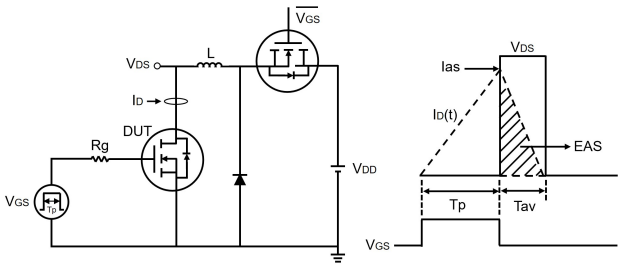


Fig16. Unclamped inductive test circuit and waveforms

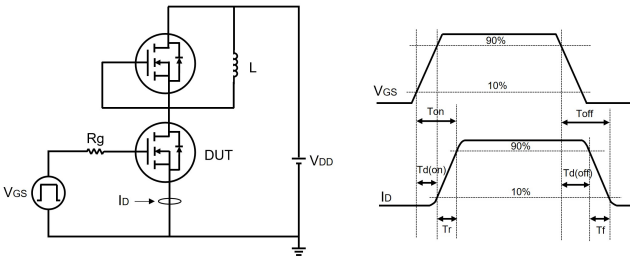
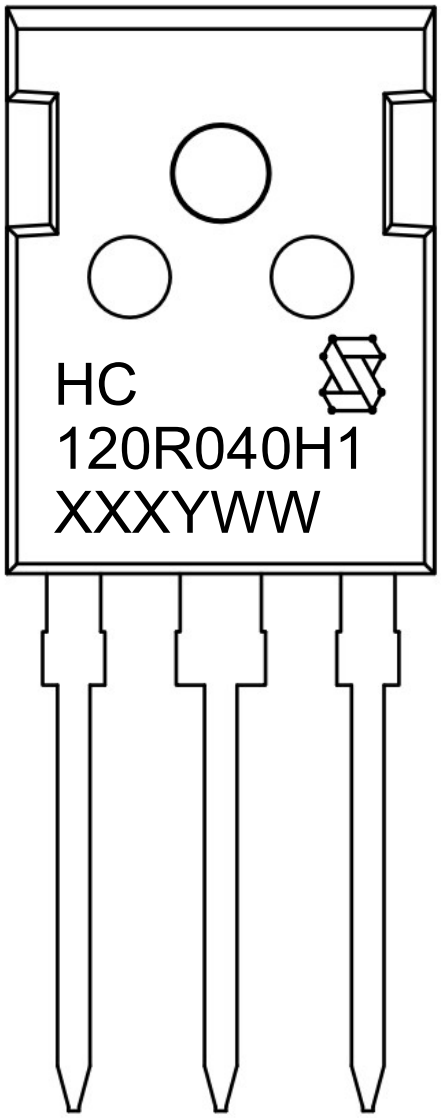


Fig17. Switching Energy Measurement Circuit

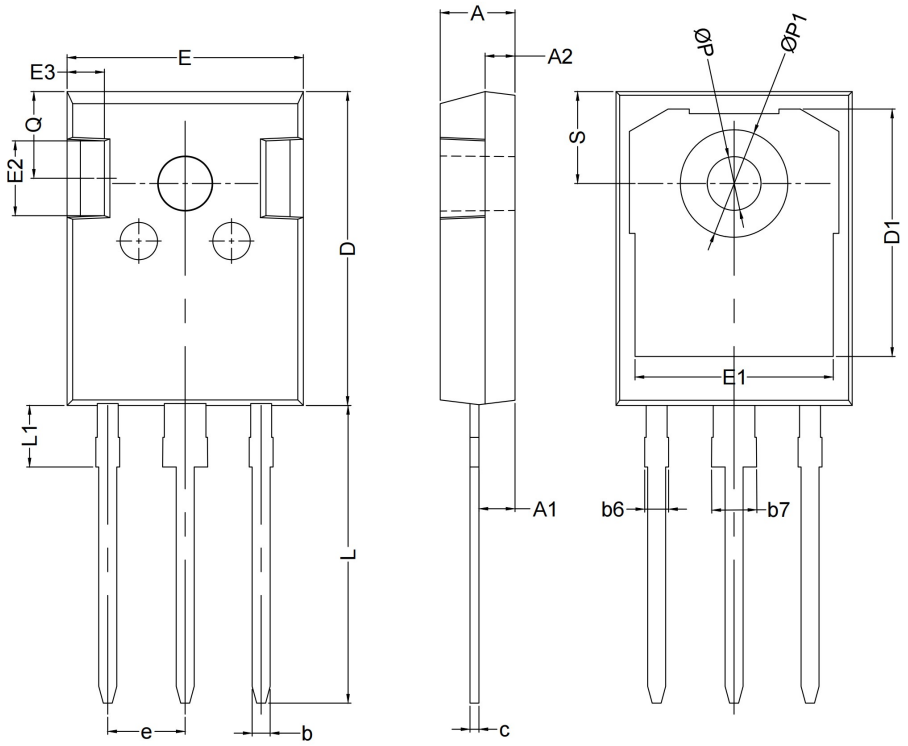
Marking Information



1st line: Vergiga Code（HC）， Vergiga Logo
2nd line: Part Number（120R040H1）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Nom	Max
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	--	1.26
b6	--	--	2.25
b7	--	--	3.25
c	0.59	--	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.40	4.50	4.60
E3	1.50	1.60	1.70
e	5.44 BSC		
L	19.80	19.92	20.10
L1	--	--	4.30
ΦP	3.40	3.50	3.60
ΦP1	7.00	--	7.40
Q	5.60	--	6.00
S	6.05	6.15	6.25

Notes:

1. Package Reference: JEDEC TO-247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.